The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first resinous substrate, and a liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface;

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising a resinous material provided over said thin film transistor,

said thin film transistor comprising:

a semiconductor layer comprising ~~a source region, a drain region, and~~ a channel formation region ~~provided between said source region and said drain region~~; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises amorphous silicon.

2. (Previously Presented) The device of claim 1 wherein said thin film transistor is an inverted-staggered thin-film transistor.

3. (Previously Presented) The device of claim 1 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

4. (Previously Presented) The device of claim 1 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid, and 2-ethylhexyl ester of acrylic acid.

5. (Currently Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first resinous substrate, and a liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising a resinous material provided over said thin-film transistor; and

at least one pixel electrode provided on said interlayer insulating layer,

said thin-film transistor comprising:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises <u>crystalline</u> silicon ~~and is obtained by crystallizing amorphous silicon~~.

6. (Previously Presented) The device of claim 5 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

7. (Previously Presented) The device of claim 5 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid,

ethyl ester of acrylic acid, butyl ester of acrylic acid, and 2-ethylhexyl ester of acrylic acid.

8. (Original) The device of claim 5 wherein said interlayer insulating layer comprises polyimide.

9.-10. (Canceled)

11. (Currently Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first resinous substrate, and a liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface;

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising a resinous material provided over said thin film transistor,

said thin film transistor comprising:

a semiconductor layer comprising ~~a source region, a drain region, and~~ a channel formation region ~~provided between said source region and said drain region~~; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises microcrystalline silicon.

12. (Currently Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first resinous substrate, and a ferroelectric liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising a resinous material provided over said thin film transistor,

said thin film transistor comprising:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises crystalline silicon ~~and is obtained by crystallizing amorphous silicon~~.

13. (Previously Presented) The device of claim 11 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

14. (Previously Presented) The device of claim 12 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

15. (Previously Presented) The device of claim 11 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid, and 2-ethylhexyl ester of acrylic acid.

16. (Previously Presented) The device of claim 12 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid, and 2-ethylhexyl ester of acrylic acid.

17. (Previously Presented) The device of claim 5 wherein said pixel electrode comprises an indium tin oxide.

18. (Currently Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first resinous substrate, and a ferroelectric liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising a resinous material provided over said thin film transistor,

said thin film transistor comprising:

a semiconductor layer comprising ~~a source region, a drain region, and~~ a channel formation region ~~provided between said source region and said drain region~~; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said channel formation region comprises amorphous silicon.

19. (Previously Presented) The device of claim 18 wherein said thin film transistor is an inverted-staggered thin-film transistor.

20. (Previously Presented) The device of claim 18 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

21. (Previously Presented) The device of claim 18 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid and 2-ethylhexyl ester of acrylic acid.

22. (Previously Presented) The device of claim 18 wherein said interlayer insulating layer comprises polyimide.

23. (Currently Amended) A semiconductor device comprising:

a resinous substrate having an uneven surface, a substrate opposed to said resinous substrate, and a ferroelectric liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and

a thin film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising a resinous material provided over said thin-film transistor;

at least one pixel electrode provided on said interlayer insulating layer,

said thin film transistor comprising:

a semiconductor layer comprising ~~a source region, a drain region, and~~ a channel formation region ~~provided between said source region and said drain region~~; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises amorphous silicon.

24. (Previously Presented) The device of claim 23 wherein said thin film transistor is an inverted-staggered thin-film transistor.

25. (Previously Presented) The device of claim 23 wherein said resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

26. (Previously Presented) The device of claim 23 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid and 2-ethylhexyl ester of acrylic acid.

27. (Previously Presented) The device of claim 23 wherein said interlayer insulating layer comprises polyimide.

28. (Currently Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first substrate, and a ferroelectric liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising a resinous material provided over said thin film transistor,

wherein said thin-film transistor comprises:

a semiconductor layer comprising ~~a source region, a drain region, and~~ a channel formation region ~~provided between said source region and said drain region~~; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween, and

wherein said channel formation region comprises microcrystalline silicon.

29. (Previously Presented) The device of claim 28 wherein said thin film transistor is an inverted-staggered thin-film transistor.

30. (Previously Presented) The device of claim 28 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

31. (Previously Presented) The device of claim 28 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid and 2-ethylhexyl ester of acrylic acid.

32. (Previously Presented) The device of claim 23 wherein said pixel electrode comprises an indium tin oxide.

33. (Currently Amended) A semiconductor device comprising:

a resinous substrate having an uneven surface, a substrate opposed to said resinous substrate, and a ferroelectric liquid crystal layer therebetween;

a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising a resinous material provided over said thin-film transistor; and

at least one pixel electrode provided on said interlayer insulating layer,

said thin-film transistor comprising:

a semiconductor layer comprising ~~a source region, a drain region, and~~ a channel formation region ~~provided between said source region and said drain region~~; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween,

wherein said semiconductor layer comprises microcrystalline silicon.

34. (Previously Presented) The device of claim 33 wherein said thin film transistor is an inverted-staggered thin-film transistor.

35. (Previously Presented) The device of claim 33 wherein said resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

36. (Previously Presented) The device of claim 33 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid and 2-ethylhexyl ester of acrylic acid.

37. (Previously Presented) The device of claim 33 wherein said pixel electrode comprises an indium tin oxide.

38. (Currently Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first resinous substrate, and a liquid crystal layer therebetween, wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface;

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising a resinous material provided over said thin film transistor,

wherein said thin film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween.

39. (Previously Presented) The device of claim 38 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid, and 2-ethylhexyl ester of acrylic acid.

40. (Currently Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, a second resinous substrate opposed to said first substrate, and a ferroelectric liquid crystal layer therebetween, wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising a resinous material provided over said thin film transistor,

said thin-film transistor comprising:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween.

41. (Previously Presented) The device of claim 40 wherein said thin film transistor is an inverted-staggered thin-film transistor.

42. (Previously Presented) The device of claim 40 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid and 2-ethylhexyl ester of acrylic acid.

43. (Previously Presented) A semiconductor device comprising:

a resinous substrate having an uneven surface, a substrate opposed to said resinous substrate, and a ferroelectric liquid crystal layer therebetween, wherein said resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide;

a resinous layer provided on said uneven surface of said resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising a resinous material provided over said thin-film transistor; and

at least one pixel electrode provided on said interlayer insulating layer,

wherein said thin-film transistor comprises:

a semiconductor layer comprising a source region, a drain region, and a channel formation region provided between said source region and said drain region; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film therebetween.

44. (Previously Presented) The device of claim 43 wherein said thin film transistor is an inverted-staggered thin-film transistor.

45. (Previously Presented) The device of claim 43 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid and 2-ethylhexyl ester of acrylic acid.

46. (Previously Presented) The device of claim 43 wherein said pixel electrode comprises an indium tin oxide.

47. (Currently Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, and a second resinous substrate opposed to said first resinous substrate;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising a resinous material provided over said thin-film transistor; and

at least one pixel electrode provided on said interlayer insulating layer,

wherein said thin-film transistor comprises:

a semiconductor layer comprising ~~a source region, a drain region, and~~ a channel formation region ~~between said source region and said drain region~~; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film interposed therebetween.

48. (Previously Presented) The device of claim 47 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

49. (Previously Presented) The device of claim 47 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid, and 2-ethylhexyl ester of acrylic acid.

50. (Previously Presented) The device of claim 47 wherein said interlayer insulating layer comprises polyimide.

51. (Previously Presented) The device of claim 47 wherein said semiconductor layer comprises silicon.

52. (Previously Presented) The device of claim 47 wherein said semiconductor device is a liquid crystal display device.

53. (Currently Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, and a second resinous substrate opposed to said first resinous substrate;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface; and

a thin-film transistor provided on said planarized surface of said resinous layer;

an interlayer insulating layer comprising a resinous material provided over said thin-film transistor; and

at least one pixel electrode provided on said interlayer insulating layer,

wherein said thin-film transistor comprises:

a semiconductor layer comprising ~~a source region, a drain region, and~~ a channel formation region ~~between said source region and said drain region~~; and

a gate electrode provided over said channel formation region with a gate insulating film interposed therebetween.

54. (Previously Presented) The device of claim 53 wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide.

55. (Previously Presented) The device of claim 53 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid, and 2-ethylhexyl ester of acrylic acid.

56. (Previously Presented) The device of claim 53 wherein said interlayer insulating layer comprises polyimide.

57. (Previously Presented) The device of claim 53 wherein said semiconductor layer comprises silicon.

58. (Previously Presented) The device of claim 53 wherein said semiconductor device is a liquid crystal display device.

59. (Currently Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, and a second resinous substrate opposed to said first resinous substrate, wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface;

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising a resinous material provided over said thin film transistor,

wherein said thin film transistor comprises:

a semiconductor layer comprising ~~a source region, a drain region, and~~ a channel formation region ~~provided between said source region and said drain region~~; and

a gate electrode provided adjacent to said channel formation region with a gate insulating film interposed therebetween.

60. (Previously Presented) The device of claim 59 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid, and 2-ethylhexyl ester of acrylic acid.

61. (Previously Presented) The device of claim 59 wherein said interlayer insulating layer comprises polyimide.

62. (Previously Presented) The device of claim 59 wherein said semiconductor layer comprises silicon.

63. (Previously Presented) The device of claim 59 wherein said semiconductor device is a liquid crystal display device.

64. (Currently Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, and a second resinous substrate opposed to said first resinous substrate, wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface;

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising a resinous material provided over said thin film transistor,

wherein said thin film transistor comprises:

a semiconductor layer comprising ~~a source region, a drain region, and~~ a channel formation region ~~provided between said source region and said drain region~~; and

a gate electrode provided over said channel formation region with a gate insulating film interposed therebetween.

65. (Previously Presented) The device of claim 64 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid, and 2-ethylhexyl ester of acrylic acid.

66. (Previously Presented) The device of claim 64 wherein said interlayer insulating layer comprises polyimide.

67. (Previously Presented) The device of claim 64 wherein said semiconductor layer comprises silicon.

68. (Previously Presented) The device of claim 64 wherein said semiconductor device is a liquid crystal display device.

69. (Currently Amended) A semiconductor device comprising:

a first resinous substrate having an uneven surface, and a second resinous substrate opposed to said first resinous substrate, wherein said first resinous substrate comprises a material selected from the group consisting of polyethylene terephthalate, polyethylene naphthalate, polyethylene sulfite and polyimide;

a resinous layer provided on said uneven surface of said first resinous substrate and having a planarized surface;

a thin film transistor provided on said planarized surface of said resinous layer; and

an interlayer insulating layer comprising a resinous material provided over said thin film transistor,

at least one pixel electrode provided on said interlayer insulating layer,

wherein said thin film transistor comprises:

a semiconductor layer comprising ~~a source region, a drain region, and~~ a channel formation region ~~provided between said source region and said drain region~~; and

a gate electrode provided over said channel formation region with a gate insulating film interposed therebetween.

70. (Previously Presented) The device of claim 69 wherein said resinous layer comprises a material selected from the group consisting of methyl ester of acrylic acid, ethyl ester of acrylic acid, butyl ester of acrylic acid, and 2-ethylhexyl ester of acrylic acid.

71. (Previously Presented) The device of claim 69 wherein said interlayer insulating layer comprises polyimide.

72. (Previously Presented) The device of claim 69 wherein said semiconductor layer comprises silicon.

73. (Previously Presented) The device of claim 69 wherein said semiconductor device is a liquid crystal display device.